ABSTRACT OF THE DISCLOSURE

A semiconductor memory is configured such that it can be connected with a first and second timing generator. The semiconductor memory includes (a) a first register configured to communicate with a memory array and the first timing generator, to retrieve and to hold first data from the memory array at a first timing, (b) a logic gate configured to communicate with the memory array and the first register, to receive the first data from the first register and second data from the memory array after the first timing, so as to compare the first and second data with each other, so that it can provide a comparison result indicating whether or not the first and second data agree with each other, and (c) a second register configured to communicate with the logic gate and the second timing generator, to retrieve and to hold the comparison result at a second timing.